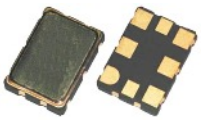
FEATURES

- **Wide frequency range**
- **Ultra low RMS Jitter**
- **Miniature packages available**



GENERAL SPECIFICATIONS at Ta = +25°C

Output Logic	CMOS	PECL	LVDS	HCSL	CML
Supply Voltage	+1.8V ±5%	--	+1.8V ±5% †	+1.8V ±5%	+1.8V ±5%
	+2.5 V ±10%	+2.5V ±10%	+2.5V ±10%	+2.5V ±10%	+2.5V ±10%
	+3.3 V ±10%	+3.3V ±10%	+3.3V ±10%	+3.3V ±10%	+3.3V ±10%
Available Frequency Range	15MHz ~ 250MHz	15MHz ~ 2,100MHz	15MHz ~ 2,100MHz	15MHz ~ 700MHz	15MHz ~ 2,100MHz
Output Load	15pF	50Ω into Vdd - 2V or Thevenin equivalent	100Ω between output and complementary output	50Ω to GND	50Ω to Vdd
Output Logic 'HIGH' '1'	Vdd - 0.4 min.	Vdd - 1.165V min. Vdd - 0.8V max.	Vdd: 1.4V typ. Vdd: 1.6V max.	Vdd: 0.66V min. Vdd: 1.15V max.	Vdd - 0.085V min. Vdd = Vdd max.
Output Logic 'LOW' '0'	Vdd x 0.1V max. 0.3V max. for 1.8V	Vdd - 2.0V min. Vdd - 1.55V max.	Vdd: 1.1V typ. Vdd: 0.9V min.	Vdd: -0.15V min. Vdd: 0.15V max.	Vdd - 0.6V min. Vdd - 0.32V max.
Current Consumption (Vdd = +3.3V)	75mA typ. 90mA max.	100mA typ. 120mA max.	75mA typ. 90mA max.	80mA typ. 100mA max.	70mA typ. 85mA max.
Current With Output Disabled	62mA typ.	99mA typ.	74mA typ.	79mA typ.	69mA typ.
Output Voltage Swing	--	595mV min. 930mV max.	250mV min. 450mV max.	450mV min. 700mV typ.	200mV min. 600mV max.
Rise/Fall Time	5ns max. (10%~90% waveform)	0.4ns max. (20%~80% waveform)	0.4ns max. (20%~80% waveform)	0.4ns max. (20%~80% waveform)	0.4ns max/ (20%~80% waveform)

Phase Jitter (12kHz to 20MHz)	156.250MHz: 159 fsec typ.; 491.520MHz: 155 fsec typ.; 644.530MHz: 151 fsec typ.; 2.000MHz: 163 fsec typ.			
Frequency Stability Codes	Frequency Stability over Operating Temp. Range	±25ppm	±50ppm	±100ppm
	Commercial *(-10° to +70°C)*	*A*	*B*	*C*
	Industrial *(-40° to +85°C)*	*D*	*E*	*F*
	Extended Industrial (-40°C to +105°C)	--	*H*	*I*
Duty Cycle	50±5%; 50±10% for 1.8V CMOS only			
Start-up Time	5.0ms typ., 10.0ms max.			
Ageing at 25°C	±3ppm max for first year; ±2ppm (max) per year thereafter			
Storage Temp. Range	-55° to +150°C			

OUTPUT ENABLE FUNCTION

OE Control on pin 1	80% of Vdd (min.) To enable output
	20% of Vdd (max.) To disable output
Output Enable Time	2.5ms max.
Output Disable Time	10.0μs max.

CONTROL VOLTAGE FUNCTION ON PAD 1

Vcontrol Centre	+0.9V for 1.8V Supply	+1.25V for 2.5V Supply	+1.65V for 3.3V Supply
Vcontrol Range	0V~+1.8V	+0.25V ~ +2.25V	+0.3 ~ +3.0V
Frequency Pulling Range	±100ppm min. ±200ppm available	±100ppm min. ±200ppm available	±100ppm min. ±200ppm available
Linearity	1% typ.; 10% max.		
Transfer Function	Positive Transfer		
Input Impedance	5MΩ min.		
Bandwidth	10kHz typ. Measured at -3dB		

† 1.8V LVDS Requires AC coupling (100nF series capacitor)

Package Drawings & Ordering Information Overleaf

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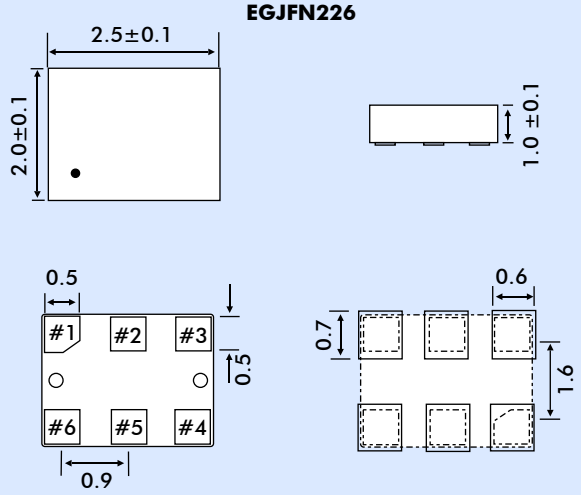
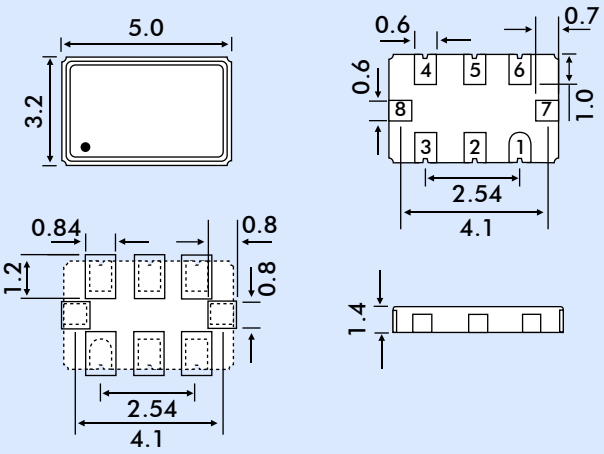
OUTLINE DIMENSIONS (Unit: mm) **SUGGESTED PAD LAYOUT FOR SMDs**

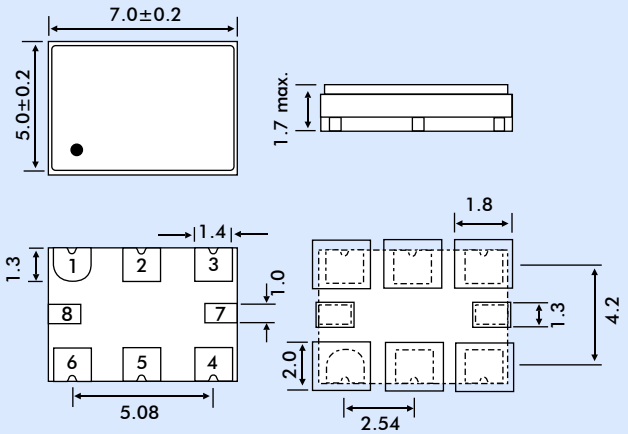
EGJFN226



EGJFN538



EGJFN578



Pad Connections

Pad 1: Control Voltage
Pad 2: Output Enable
Pad 3: Ground
Pad 4: CMOS: Output, Differential: Output
Pad 5: CMOS: NC Differential: Complementary Output
Pad 6: Supply Voltage
Pads 7, 8: No Connection

PART NUMBER FORMAT AND EXAMPLE

Example: 25 EGDJFN 226 - E - 150N 120.000

Supply Voltage
18 = 1.8 Volts
25 = 2.5 Volts
3 = 3.3 Volts

Output Type
T = CMOS
P = LVPECL
D = LVDS
C = HCSL
Q = CML

Package
578 = 7.0 x 5.0mm
538 = 5.0 x 3.2mm
226 = 2.5 x 2.0mm

Frequency Stability
See Codes on Page 1

Freq. Pulling Range
150 = ±150ppm
N = minimum
M = maximum
T = typical

Frequency in MHz

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