LVDS

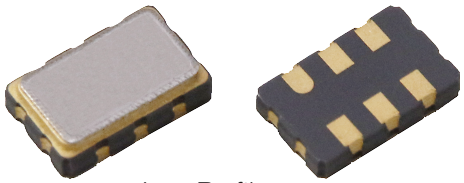
LVDS Output

10 MHz to 160 MHz

Differential Output Crystal Oscillator

DESCRIPTION

Statek's surface mount Low Voltage Differential Output Crystal Oscillators are designed for applications requiring ultra high frequency differential outputs, superior phase noise performance, and low jitter in a small footprint.



Low Profile

FEATURES

- High shock option
- Low phase noise and low phase jitter
- Available at 2.5 V and 3.3 V operating voltages
- Low Allan deviation without PLL artifacts
- High frequency fundamental mode crystal
- Ultra-low period jitter

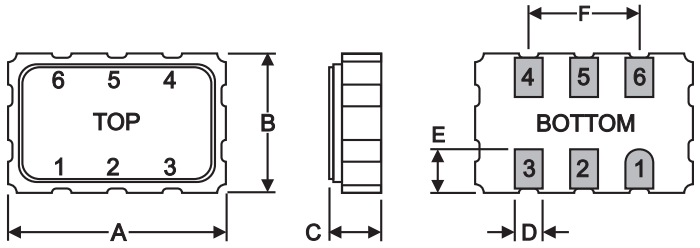
APPLICATIONS

- Avionics
- Communications
- Guidance and Navigation

PIN CONNECTIONS

1. Enable/Disable (E) or not connected (N)
2. Not Connected (NC)
3. Ground
4. LVDS
5. LVDS (complementary)
6. Supply Voltage (V_{DD})

PACKAGE DIMENSIONS



DIM	Termination	LVDSA	LVDSB
		Typical (mm)	
A		7.00	5.00
B		5.00	3.20
C	SM1	1.50	1.30
	SM3/SM5	1.60	1.40
D		1.40	0.64
E		1.10	1.20
F		5.08	2.54

PACKAGING OPTIONS

LVDS - Tray Pack

- Tape and reel Per EIA 481

HOW TO ORDER LVDS SURFACE MOUNT CRYSTAL OSCILLATORS

LVDS B HGD 4 S E – 125.0M , 50 / 50 / — / I

- **B** — Package Size: A = 5.0 x 7.0 mm; B = 5.0 x 3.2 mm
- **4** — Supply Voltage: 2 = 2.5 V; 4 = 3.3 V
- **E** — Enable/Disable: Option E or N
- **–** — Terminations: Blank = Gold Plated (Pb Free); SM3 = Solder Dipped; SM5 = Solder Dipped (Pb Free)
- **125.0M** — Frequency: M = MHz
- **50** — Calibration Tolerance @ 25°C (in ppm)
- **50** — Frequency Stability over Temp. Range (in ppm)
- **I** — Temperature Range: C = -10°C to +70°C; I = -40°C to +85°C; M = -55°C to +125°C; S = Customer Specified
- **HGD** — Blank = 5,000 g (standard); HGC = 20,000 g; HGD = 30,000 g
- **S** — Special or Custom: Blank = Standard; S = Special or Custom

OR

— / — / 100 / I

- **100** — Total Frequency Tolerance (in ppm)
- **I** — Temperature Range: C = -10°C to +70°C; I = -40°C to +85°C; M = -55°C to +125°C; S = Customer Specified

10231 Rev D

STATEK CORPORATION 512 N. MAIN ST., ORANGE, CA 92868 714-639-7810 FAX: 714-997-1256 www.statek.com

ENABLE/DISABLE OPTIONS (E/N)

Statek offers two enable/disable options: E and N. The E-version has a tri-state output and stops oscillating internally when the output is put into the high Z state. The N-version does not have PIN 1 connected internally and so has no enable/disable capability. The following table describes the Enable/Disable option E.

ENABLE/DISABLE OPTION E FUNCTION TABLE

	Enable (Pin 1 High*)	Disable (Pin 1 Low)
Output	Frequency Output	High Z State
Oscillator	Oscillates	Stops
Current	Normal	Very Low

*When PIN 1 is allowed to float, it is held high by an internal pull-up resistor.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD}	-0.3 V to 4.0 V
Storage Temperature	-55°C to +150°C
Maximum Process Temperature	260°C for 10 seconds
ESD Protection Human Body Model	2 kV

SPECIFICATION TABLES

Parameters listed are at 25°C unless otherwise noted.

Parameter	Symbol	Units	Tightest	Standard	Maximum	Conditions / Comments
Frequency		MHz		10 to 160		
Supply Voltage		V		3.3 ±10%		2.5 ±10% available
Calibration Tolerance		ppm	±25	±50	±100	At 25°C Other tolerances available
Frequency Stability[1]		ppm	±50	±75	±100	-55°C to +125°C
		ppm	±30	±50	±100	-40°C to +85°C
Frequency Tolerance (Total)		ppm	±40	±50	±100	-40°C to +85°C
Shock, survival[2]		g			5,000	0.3 ms, ½ sine: LVDSA
		g			30,000	0.3 ms, ½ sine: LVDSB
Vibration, survival[3]		g		20		10-2,000 Hz swept sine
Aging		ppm		±5		First year depending on frequency

LVDS Output Parameter	Symbol	Units	Minimum	Typical	Maximum	Conditions / Comments
Output Differential Voltage	V_{OD}	mV	247	330	454	RL = 100 Ω (1%) See Figure 1
Output Differential Voltage Error	ΔV_{OD}	mV			50	
Output High Voltage	V_{OH}	V		1.4	1.6	
Output Low Voltage	V_{OL}	V	0.9	1.1		
Offset Voltage	V_{OS}	V	1.125	1.250	1.375	
Offset Voltage Error	ΔV_{OS}	mV	0		50	
Output Leakage	I_{OS}	uA			10	V_{OUT} = V_{DD} or GND (OE=0V)
Stand by Current	I_{OSD}	uA			15	Ta ≤ +85°C
					30	Ta > +85°C
Rise Time (Differential Clock)	t_R	ps		200		RL = 100 Ω (20% to 80%)
Fall Time (Differential Clock)	t_F	ps		200		See Figures 2 and 3
Supply Current (Outputs Loaded)[4]	I_{DD}	mA		25	30	
Duty Cycle (Output Clock)[5]		%	40		60	At Differential 0V. See Figures 2 and 3.
Output Swing	V_{DIFF}	V	0.4			See Figure 2

Timing Jitter - 125 MHz	Symbol	Units	Minimum	Typical	Maximum	Conditions / Comments
Jitter (Integrated)		ps		0.053		125 MHz (12 kHz to 20 MHz RMS)
Jitter (Period)		ps		1.0		125 MHz (10,000 cycles RMS)

Phase Noise - 125 MHz	Symbol	Units	1 kHz offset	10 kHz offset	100 kHz offset	20 MHz offset	40 MHz offset
Typical (LVDS)	$\mathscr{L}$	dBc/Hz	-132	-149	-155	-165	-166

1. Does not include calibration tolerance.
2. Shock survival 10 MHz - 125 MHz.
3. Per MIL-STD-202G, Method 204D, Random vibration testing also available.
4. Typical for 160 MHz, 3.3 V.
5. Contact factory for 45-55% duty cycle.

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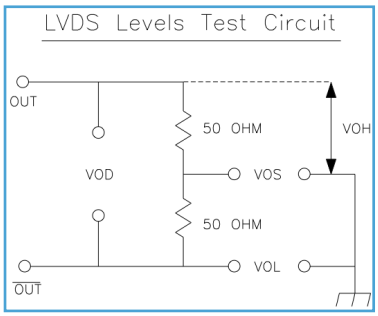


Figure 1

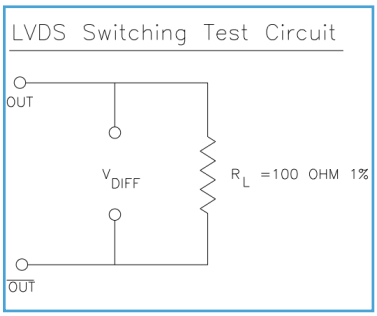


Figure 2

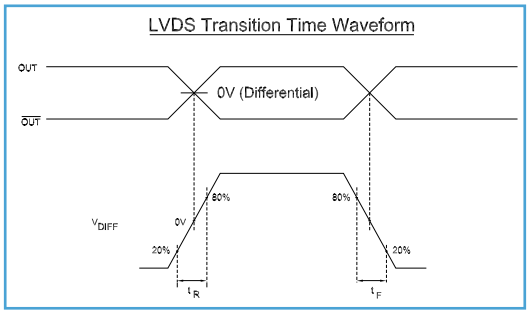
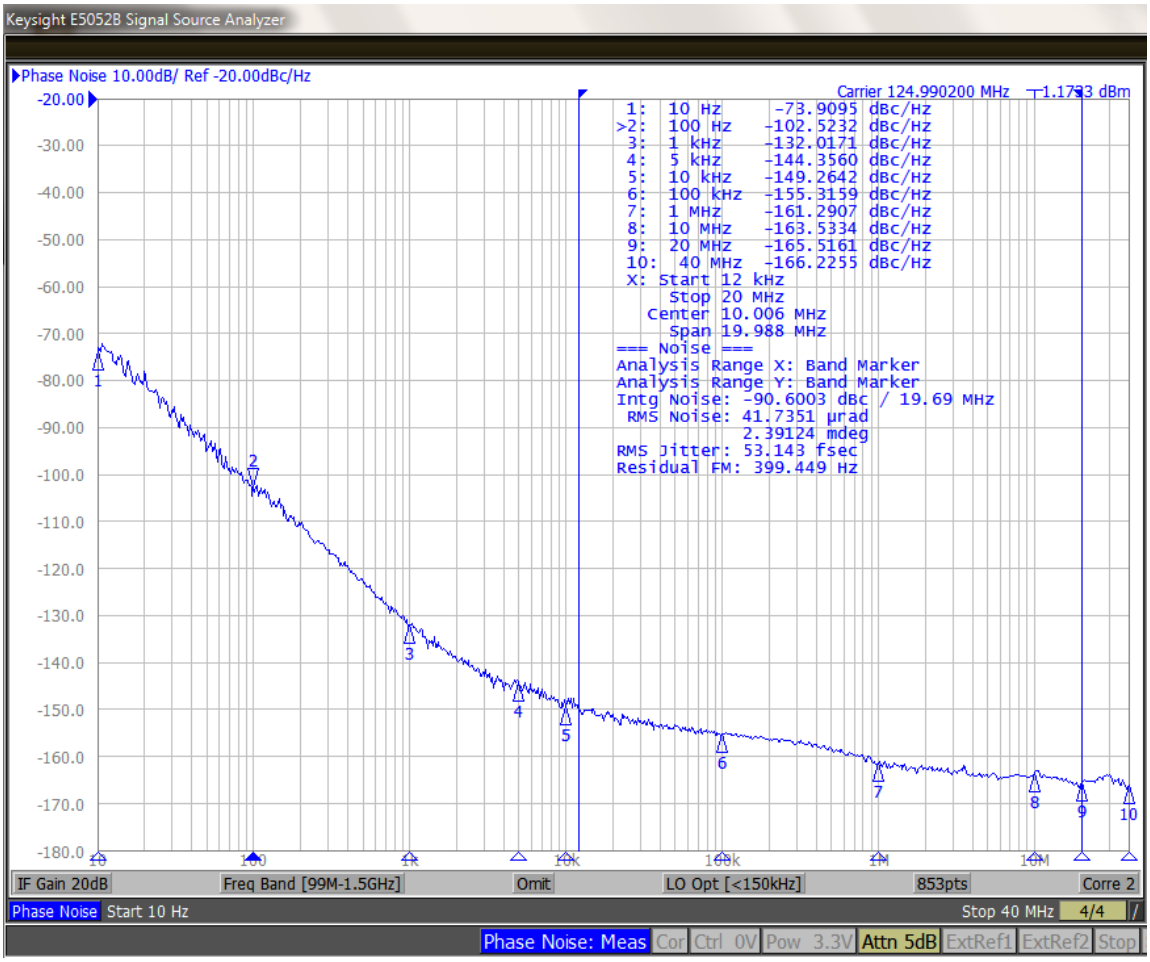


Figure 3

PHASE NOISE PERFORMANCE AT 125 MHZ



Jitter (Integrated) 53 fsec Typical

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