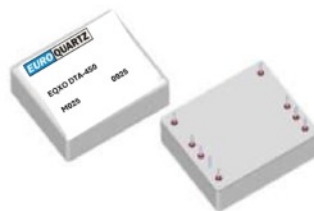


- Low power consumption
- 1pps input and output for timing synchronization
- ToD (Time of Day)
- RS232 digital interface


**GENERAL SPECIFICATION**

Frequency	10.000MHz
Output Waveform	3.3V CMOS
Load Impedance	1MΩ
Rise/Fall Time	10ns max.
Output Logic 'High'	2.2V min.
Output Logic 'Low'	0.7V max.
Short Term (ADEV)	0.3ppb max. @ Tau = 1sec
	0.1ppb max. @ Tau = 10sec
	0.03ppb max. @ Tau = 100sec
Duty Cycle	50±5%
Frequency Stability Over Temperature	±1ppb max. (-10°C to 70°C, Temperature Slope <0.5°C/min)
Frequency Accuracy	±0.05ppb max.
Daily Aging	±0.03ppb max.
Frequency Control (Resolution = $1 \times 10^{-12}$ , Vcon = 0V~2.5V)	±20ppb min.

**1pps Time Output**

1pps	10Hz
Output Amplitude	3.3V LVTTTL
Pulse Width	1ms min.
Rise/Fall Time	10ns max.
Load	1MΩ

**Built-In Test Equipment (BITE) Output**

Format	3.3V
Load Impedance	1MΩ
Logic	0 = Normal Operation 1 = Alarm

**Supply Voltage**

Supply Voltage	3.3±0.1Vdc
Steady Power	130mW max.
Warm-up Power	200mW max.
Warm-up Time	180 sec. max.

**Digital Communication**

Storage Temperature	-55°C to +85°C
Vibration	Lock Under Below: 20Hz~80Hz, +3dB/oct; 80Hz~350Hz, 0.4g <sup>2</sup> /Hz; 350Hz~2000Hz, -3dB/oct; 6.06g RMS
Humidity	0-95%, RH
Magnetic Sensitivity	< +9x10 <sup>-11</sup> /Gauss

**1pps Time Input**

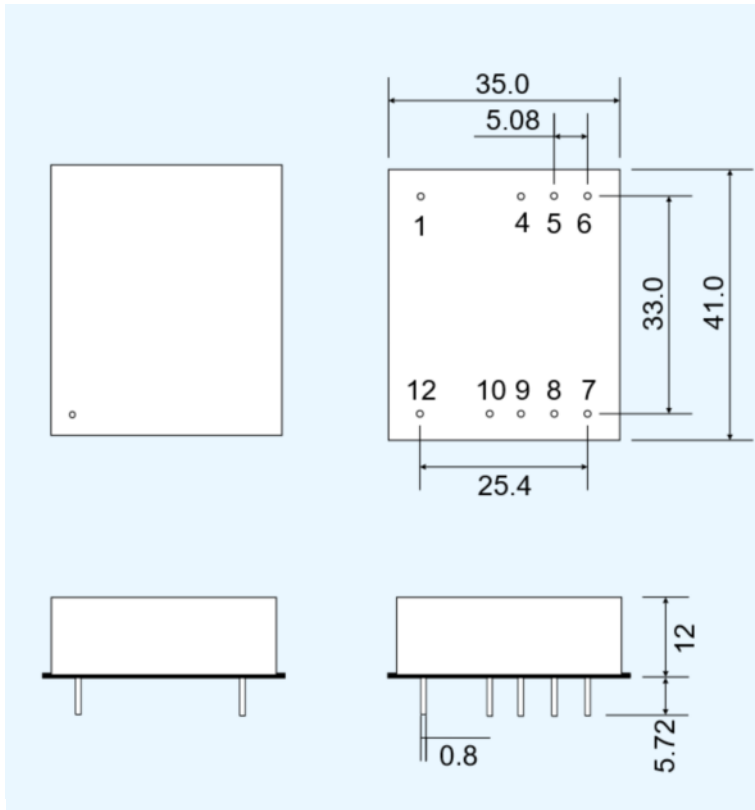
1pps	1Hz
Timing Edge	Rising Edge
Low Level	0.7V max.
High Level	2.2V min.

**Phase Noise @10MHz**

Offset	Phase Noise
1Hz	-55dBc/Hz
10Hz	-80dBc/Hz
100Hz	-113dBc/Hz
1kHz	-125dBc/Hz
10kHz	-135dBc/Hz

**Digital Communication**

Protocol	RS202
Logic Level	LVTTTL
Baud Rate	57600
Number of Data Bits	8
Number of Stop Bits	1
Parity	None

Pin Connections

Pin 1: Tune  
Pin 4: BITE  
Pin 5: TX  
Pin 6: RX  
Pin 7: Vcc  
Pin 8: GND  
Pin 9: 1pps in  
Pin 10: 1pps out  
Pin 12: 10MHz out

**Ordering Part Number****EQXO-DTA450**