Differential Output (VC)TCXO 15MHz to 2100MHz

- **0.8pS RMS integrated phase jitter**
- **Miniature package sizes**
- **Supply voltage 1.8V, 2.5V or 3.3 VDC**
- **Frequency stability from ±1ppm over -40 to +85°C**
- **Differential Outputs and CMOS available**

DESCRIPTION

(V)EMJF series TCXOs are packaged in miniature SMD packages, available in 6 pad 3.2x2.5mm, or 8 pad 5.0x3.2mm packages. With characteristic low current consumption, and integrated phase jitter performance of 0.8 pS RMS.

GENERAL SPECIFICATION

Output Logic	HCSL	PECL	CML	LVDS
Packages	(V)EMJF326C, (V)EMJF538C	(V)EMJF326P, (V)EMJF538P	(V)EMJF326Q, (V)EMJF538Q	(V)EMJF326D, (V)EMJF538D
Supply Voltage, Vdd	+1.8V±5%, +2.5V±10%, +3.3V±10%	+2.5V±10% or +3.3V±10%	+1.8V±5%, +2.5±10%, +3.3V±10%	+1.8V±5%†, +2.5V±10%, +3.3V±10%
Frequency Range	15MHz~700MHz	15MHz~2,100MHz	15MHz~2,100MHz	15MHz~2,100MHz
Output Load	50Ω to Ground	100Ω into Vcc-2V, or Thévenin Equivalent	50Ω to Vdd	100Ω between output and complimentary output
Output Logic 'High'	Vdd: 0.66V (min.) Vdd: 1.15V (max.)	Vdd-1.03 (min.) Vdd-0.6 (max.)	Vdd-0.085V (min.) Vdd: Supply (max.)	1.4V (typ.) 1.6V (max.)
Output Logic 'Low'	Vdd: -0.15V (min.) Vdd: 0.15V (max.)	Vdd-1.85 (min.) Vdd-1.6 (max.)	Vdd-0.6V (min.) Vdd-0.32V (max.)	1.1V (typ.) 0.9V (max.)
Output Voltage Swing	620mV (min.) 700mV (min.)	595mV (min.) 930mV (max.)	200mV (min.) 600mV (min.)	250mV (min.) 450mV (max.)
Current Consumption @Vdd=+3.3V	80mA (typ.) 100mA (max.)	100mA (typ.) 120mA (max.)	70mA (typ.) 85mA (max.)	75mA (typ.) 90mA (max.)
Current With Output Disabled	79mA (typ.)	99mA (typ.)	69mA (typ.)	74mA (typ.)
Rise/Fall Time	0.4nsec. (max.) Tr/Tf: 20% to 80% of waveform			

Initial Calibration Tolerance	±1.0ppm (max.) at +25±2°C	
Frequeny Stability	Temperature	±1.5ppm over -40°C +85°C standard, ±1.0ppm available
	Aging @+25°C	±1.0ppm (max.) per year
	Voltage Change	±0.2ppm (max.) for a ±5% input voltage change
	Load Change	±0.2ppm (max.), for a ±10% load condition change
	Reflow	±1.0ppm (max.), 1 reflow and measured 24hrs afterwards
Duty Cycle	50±5%	
Start-up Time	5msec. (typ.), 10mesc. (max.)	
Storage Temperature	-55°C to 125°C	
RMS Jitter [12kHz ~ 20MHz]	15MHz~50MHz: 500fsec. (typ.); 51MHz~1,200MHz: 250fsec. (typ.)	

VOLTAGE CONTROL FUNCTION

Control Voltage Function on Pad 1	
Control Voltage Centre and Range	+1.5±1.0V for Vdd = 2.5V or 3.3V
	+0.9±0.6V for Vdd = 1.8V
Frequency Pulling Range	±8ppm (min.)
Linearity	1% (typ.); 10%(max.)
Transfer Function	Positive Transfer
Input Impedance	5MΩ (typ.)

Output Enable Function on Pad 2	
OE Control on Pad 2	70% of Vdd (min.) to enable output (Do not leave open)
	30% of Vdd (max.) to disable output
Output Enable TIme	2.5msec. (max.)
Output Disable Time	10usec. (max.)

†1.8V LVDS output requires AC coupling using 100nF series capacitor.

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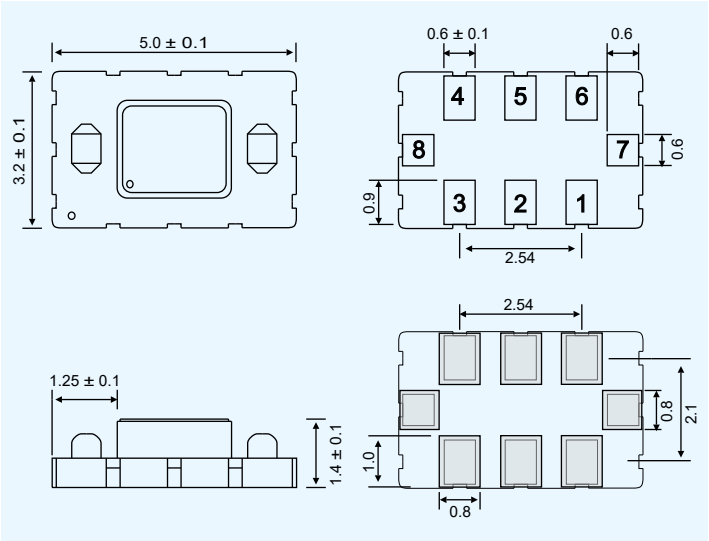
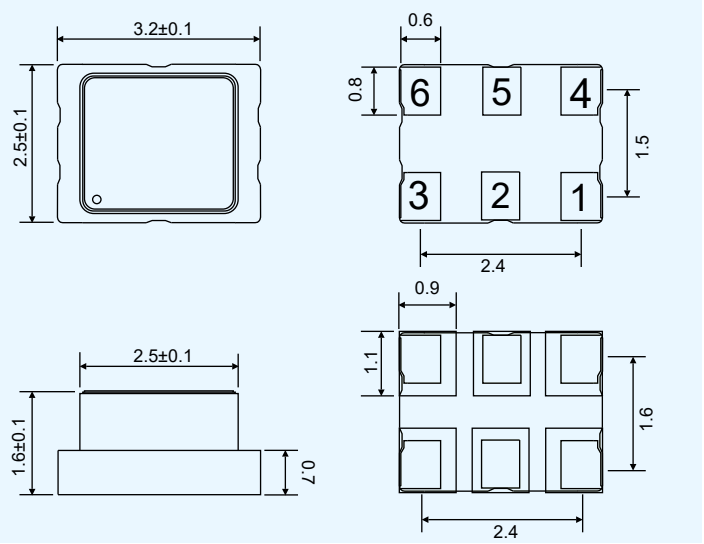
OUTLINES AND DIMENSIONS

(V)EMJF538_



Pad Connection
Pad 1: TCXO: No Connection
VCTCXO: Control Voltage
Pad 2: Enable/Disable
Pad 3: Ground
Pad 4: Output
Pad 5: Complimentary Output
Pad 6: Supply Voltage
Pads 7&8: No Connection

(V)EMJF326_



Pad Connection
Pad 1: TCXO: No Connection
VCTCXO: Control Voltage
Pad 2: Enable/Disable
Pad 3: Ground
Pad 4: Output
Pad 5: Complimentary Output
Pad 6: Supply Voltage

PART NUMBERS

Example: **VEMJF538P33-50.000-1.0/-40+85**

Series Description
TCXO = EMJF
VCTCXO = VEMJF

Package Size
538: 5.0x7.0mm
326: 3.2x2.5mm

Output Type
P = LVPECL
D = LVDS
Q = CML
C = HCSL

Supply Voltage
3.3V = 33
2.5V = 25
1.8V = 18

Frequency (MHz)

Stability over OTR (±ppm)

Operating Temperature Range (OTR) (°C)

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